Listing of the Claims

A complete listing of the claims with proper claim identifiers is set forth below.

1. (Currently amended). An integrated read-only memory, comprising:

having selection transistors, each selection transistors having a drain connection[[,]];

having an electrode for feeding a voltage or a current[[,]];

having a layer between the drain connections and the electrode electrically linking the drain connections to the electrode, the electrical resistance of which the layer can be changed through the effect of a configuration voltage or a configuration current[[,]];

having a source connection per selection transistor[[,]]; and

having a bit line that is electrically connected to at least one source connection,

in which the layer is formed as a common layer for linking the drain connections to the electrode, and

in which the electrical resistance of the layer can be changed locally.

2. (Currently amended). The read-only memory as claimed in of claim 1, in which wherein the resistance of the layer can be switched over.

3. (Currently amended). The read-only memory as claimed in of claim 1 or 2, in which wherein the resistance of the layer can be switched over between two resistance characteristic curves.

4. (Currently amended). The read-only memory of as claimed in one of the preceding claims 1, further comprising:

having a read voltage applied to the layer or a read current fed to the layer within a defined voltage or current range in a read Operation of the read-only memory, and

having a configuration voltage or a configuration current outside the voltage or current range provided for the read Operation in a configuration operation of the read-only memory.

5. (Currently amended). The read-only memory of ~~as claimed in one of the preceding~~ claims 1, wherein the read-only memory ~~which~~ is designed as a flash memory.

6. (Currently amended). The read-only memory of ~~as claimed in one of the preceding~~ claims 1, ~~in which~~ wherein the selection transistors are arranged in an array.

7. (Currently amended). The read-only memory ~~as claimed in one~~ of claims 1 ~~to 6~~, ~~in which~~ wherein the bit line is connected to a decoder circuit.

8. (Currently amended). The read-only memory ~~as claimed in one~~ of claims 1 ~~to 7~~, ~~in which~~ wherein the bit line is accessible for an external connection.

9. (Currently amended). The read-only memory of ~~as claimed in one of the preceding~~ claims 1, further comprising:

~~having~~ a gate connection per selection transistor, and

~~having~~ a word line that is electrically connected to at least one gate connection.

10. (Currently amended). The read-only memory ~~as claimed in~~ of claim 9, ~~in which~~ wherein the word line is connected to a decoder circuit.

11. (Currently amended). The read-only memory ~~as claimed in~~ of claim 9 ~~or claim 10~~, ~~in which~~ wherein the word line is accessible for an external connection.

12. (Currently amended). The read-only memory of ~~as claimed in one of the preceding~~ claims 1, ~~in which~~ wherein the selection transistors have a planar construction in the substrate.

13. (Currently amended). The read-only memory ~~as claimed in one~~ of claims 1 ~~to 11~~, ~~in which~~ wherein the selection transistors have a vertical construction in the Substrate.

14. (Currently amended). The read-only memory of ~~as claimed in one of the preceding~~ claims 1, ~~in which~~ wherein the layer is formed as a molecular layer.

15. (Currently amended). The read-only memory ~~as claimed in~~ of claim 14, ~~in which~~ wherein the layer contains rotaxane.

16. (Currently amended). The read-only memory ~~as claimed in~~ of claim 14, ~~in which~~ wherein the layer contains catenane.

17. (Currently amended). The read-only memory ~~as claimed in~~ of claim 14, ~~in which~~ wherein the layer contains a bispyridinium compound.

18. (Currently amended). The read-only memory ~~as claimed in one~~ of claims 1 ~~to 13~~, ~~in which~~ wherein the layer is formed as a dielectric.

19. (Currently amended). The read-only memory ~~as claimed in~~ of claim 18, ~~in which~~ wherein the layer contains $SrZrO_3$.

20. (Currently amended). The read-only memory ~~as claimed in one~~ of claims 1 ~~to 13~~, ~~in which~~ wherein the layer is formed as a polymer.

21. (Currently amended). The read-only memory ~~as claimed in~~ of claim 20, ~~in which~~ wherein the layer contains 3-nitrobenzal malonitrile, 1,4-phenylenediamine complex.

22. (Currently amended). The read-only memory ~~as claimed in~~ of claim 20, ~~in which~~ wherein the layer contains a chalcogenide compound.

23. (Currently amended). A method for operating an integrated read-only memory comprising selection transistors, each selection transistors having a drain connection; an electrode for feeding a voltage or a current; a layer between the drain connections and the electrode electrically linking the drain connections to the electrode, the electrical resistance of the layer can be changed through a configuration voltage or a configuration current; a source connection per selection transistor; and a bit line that is electrically connected to at least one source connection ~~as claimed in one of the preceding claims~~, the method comprising:

applying, ~~in which~~ in a read operation, a read voltage or a read current within a defined voltage or current range ~~is applied~~ to the layer[[,]]; and

~~in which~~ appying, in a configuration operation, a configuration voltage or a configuration current outside the voltage or current range provided for the read operation ~~is applied~~ to the layer.

24. (Currently amended). A method for producing an integrated read-only memory, the method comprises:

~~in which~~ producing ~~an array of~~ selection transistors ~~is produced using CMOS technology~~, each selection ~~transistors~~ transistor having a drain contact ~~in which drain contacts of the selection transistors are led to the surface of the arrangement,~~;

arranging an electrode;

~~in which~~ providing a layer ~~is deposited~~ between the drain connections and the electrode electrically linking the drain connections to the electrode, the ~~whose~~ electrical resistance of the layer can be changed through ~~the effect of~~ a configuration voltage or a configuration current~~, it being possible for the electrical resistance of the layer to be changed locally,~~;

~~in which an electrode is arranged above the layer,~~

~~in which~~ forming a source connection ~~is formed~~ per selection transistor[[,]]; and

~~in which~~ forming a bit line ~~is formed~~ which is electrically connected to at least one source connection~~,~~

~~in which the layer is formed as a common layer for linking the drain connections to the electrode~~.

25. (Currently amended). The method for producing an integrated read-only memory ~~as claimed in~~of claim 24, ~~in which~~ wherein the layer is deposited as a common layer for linking the drain connections to the electrode above the selection transistors.

26. (Currently amended). The method for producing an integrated read-only memory ~~as claimed in~~ of claim 24 ~~or claim 25~~, ~~in which~~ wherein the selection transistors are produced in a front end process.

27. (Currently amended). The method for producing an integrated read-only memory ~~as claimed in one~~ of claims ~~24 to 26~~, ~~in which~~ wherein the layer is deposited in a back end process.

28. (Currently amended). The method for producing an integrated read-only memory ~~as claimed in one~~ of claims ~~24 to 27~~, ~~in which~~ wherein the selection transistors are constructed in planar fashion in the substrate.

29. (Currently amended). The method for producing an integrated read-only memory ~~as claimed in one~~ of claims 24 ~~to 27~~, ~~in which~~ wherein the selection transistors are constructed vertically in the substrate.

30. (Currently amended). The method for producing an integrated read-only memory ~~as claimed in one~~ of claims 24 ~~to 29~~, ~~in which~~ wherein the layer is formed as a molecular layer.

31. (Currently amended). The method for producing an integrated read-only memory ~~as claimed in~~ of claim 30, ~~in which~~ wherein the layer contains rotaxane.

32. (Currently amended). The method for producing an integrated read-only memory ~~as claimed in~~ of claim 30, ~~in which~~ wherein the layer contains catenane.

33. (Currently amended). The method for producing an integrated read-only memory ~~as claimed in~~ of claim 30, ~~in which~~ wherein the layer contains a bispyridinium compound.

34. (Currently amended). The method for producing an integrated read-only memory ~~as claimed in one~~ of claims 24 ~~to 29~~, ~~in which~~ wherein the layer is formed as a dielectric.

35. (Currently amended). The method for producing an integrated read-only memory ~~as claimed in~~ of claim 34, ~~in which~~ wherein the layer contains $SrZrO_3$.

36. (Currently amended). The method for producing an integrated read-only memory ~~as claimed in one~~ of claims ~~24 to 29~~, ~~in which~~ wherein the layer is formed as a polymer.

37. (Currently amended). The method for producing an integrated read-only memory ~~as claimed in~~ of claim 36, ~~in which~~ wherein the layer contains a 3-nitrobenzal malonitrile, 1.4-phenylenediamine complex.

38. (Currently amended). The method for producing an integrated read-only memory ~~as claimed in one~~ of claim~~s 24 to~~ 29, ~~in which~~ wherein the layer contains a chalcogenide compound.

39. (New). The method for producing an integrated of claim 24, wherein the selection transistors are produced using CMOS technology.